Serially-Controlled 8-Channel Analog Switch Array Simplifies Signal Conditioning and Routing

When analog signals are processed in a digital system, some of the processing must be performed in the analog domain, both before and after the digital portion of the system. CMOS analog switches are frequently used in a variety of analog signal conditioning functions under digital control, such as gain ranging, anti-aliasing filter corner-frequency selection, sample-and-hold functions, input channel selection, input summing, and signal routing.

A new serially-controlled array of precision CMOS switches simplifies the design of these functions, while improving system accuracy and reducing component count and board space. This application note presents simplified solutions for some of these digitally controlled analog signal processing circuits using the new DG485 eight-channel serially-controlled switch array.

The DG485 Switch Array

CMOS analog switches typically come in single, dual, and quad configurations. CMOS multiplexers combine up to sixteen switches on a chip, with decoding logic that allows the selection of one switch at a time. Now there is a new function that combines the best of both types of devices. The DG485 has eight switches on a chip, and through a unique serial data control architecture, any combination of the eight switches can be connected to a common output line.

A New Way to Control a Switch Array

The internal block diagram for the DG485 is shown in Figure 1. It consists of five elements: (1) the logic input stages, (2) an array of eight D-type flip-flops that form an input shift register, (3) an array of eight data latches, (4) eight switch drivers, and (5) eight CMOS analog switches. There are three power supply inputs and a ground. The three supplies are V+, V–, and V_L. V+ and V– set the analog range for the signals being controlled by the switches. The range of operation for V+ and V– is ± 5 V to ± 20 V and also includes single-supply operation by connecting V– to ground. The V_L input determines the logic switching threshold recognized by the logic input buffer stages. The nominal operating value for V_L should be 5 V to allow for TTL-compatible operation ($V_{INL} \leq 0.8$, $V_{INH} \geq 2.4$ V). However, V_L can be operated anywhere from 5 to 40 V to facilitate compatibility with a wide range of logic levels. The GND, although being the only ground point on the device, is generally considered to be a digital ground, rather than an analog ground, for the purpose of avoiding ground loops.

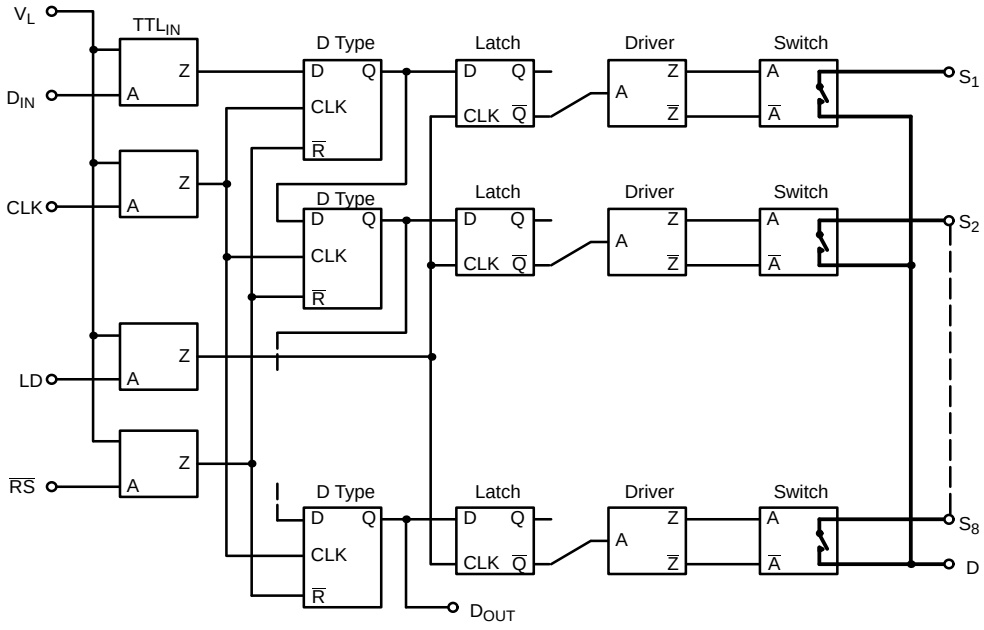


FIGURE 1. The DG485 Internal Block Diagram

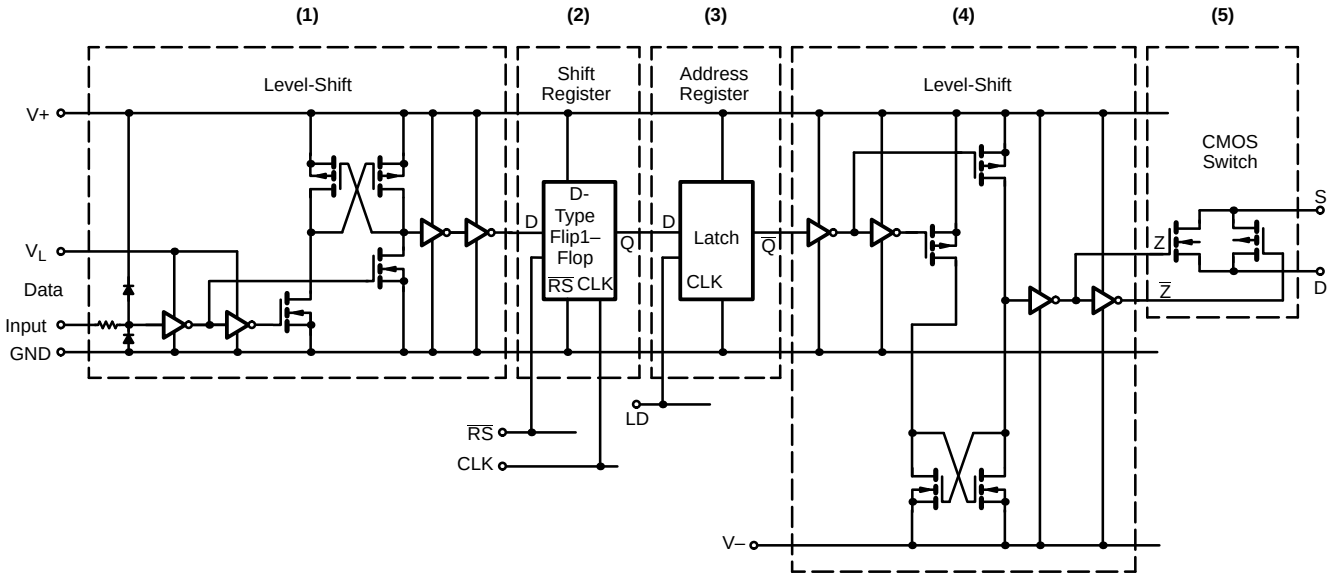


FIGURE 2. Simplified Schematic of a Typical DG485 Channel

A simplified schematic of a typical DG485 channel which details its five elements is shown in Figure 2.

The input buffer stages (1) are CMOS inverters which have ESD protection consisting of catch diodes and a resistor to dissipate the energy generated by electrostatic discharge, which can destroy an MOS input. The scheme used in the DG485 provides protection in excess of ±4000 V on all pins of the device. (This protection is required only on the logic inputs because the power supply and output connections have built-in protection via the large parasitic p-n junctions.) The TTL input buffers are CMOS inverter stages that swing between V_L and GND, and drive a level shift stage to drive the D-type master-slave flip flops (2) that swing from V+ to GND. The D-type flip-flops have master-slave inverters with edge-sensitive clocking, and they form the data input shift register. Their outputs are connected to the address register latches (3), which are single-stage clocked-inverter flip-flops with level-sensitive clocking. These latches, in turn, are connected to the switch drivers (4), which provide level translation from the latch outputs, which swing between V+ and GND, to the gates of the CMOS switches (5), which must swing from rail to rail. These switches are pairs of large p-channel MOSFETs in parallel with complementary n-channel MOSFETs; this parallel combination has a low on-resistance of 85 Ω: (maximum at 25°C). The p-channel device is turned on by driving its gate to the V– rail, and it is turned off by driving its gate to the V+ rail. In an opposite manner, the n-channel device is turned on by driving its gate to V+ and turned off by driving its gate to V–. These parallel switches compensate for each other's increase in on-resistance as the analog signal approaches either rail. That is, as the V_{GS} for one device goes to zero, it shuts off, while the opposite polarity device is fully enhanced or turned on hard. The result is a fairly flat on-resistance as the analog voltage of the source (or drain) ranges from V+ to V–. Typically, a ±8 Ω variation is seen.

Controlling the Array with a Serial Data Bus

The DG485 connects to the serial output of a microprocessor system, as shown in Figure 3. The eight CMOS switches in the DG485 are controlled via the serial data output via the D_{IN} (data in) pin. Data is loaded into the eight-bit shift register with each clock pulse at the CLK (clock) input. The contents of the shift register are loaded into the octal latch when a logic "high" signal is applied to the LD (load) input. The octal latch holds the state (on or off) of the individual switches in the array. The $\overline{RS}$ (reset) input resets the octal latch to all "zeroes" when a logic "low" is applied, turning all switches off with a subsequent LD command.

Analog-Signal Voltage Ranges

The power supplies for the device are V+, V–, and V_L. The analog signal range of the switches is defined by the power supply rails. Because the DG485 is built on a 44 V silicon-gate CMOS process, rail-to-rail signal swings are possible. The power supply voltages range from ±5 V to ±20 V, and single-supply operation is allowed from +5 V to +40 V. The logic levels are set with V_L input. With 5 V applied to V_L, TTL and 5 V CMOS logic compatibility (V_{INL} = 0.8 V, V_{INH} = 2.4 V) is assured.

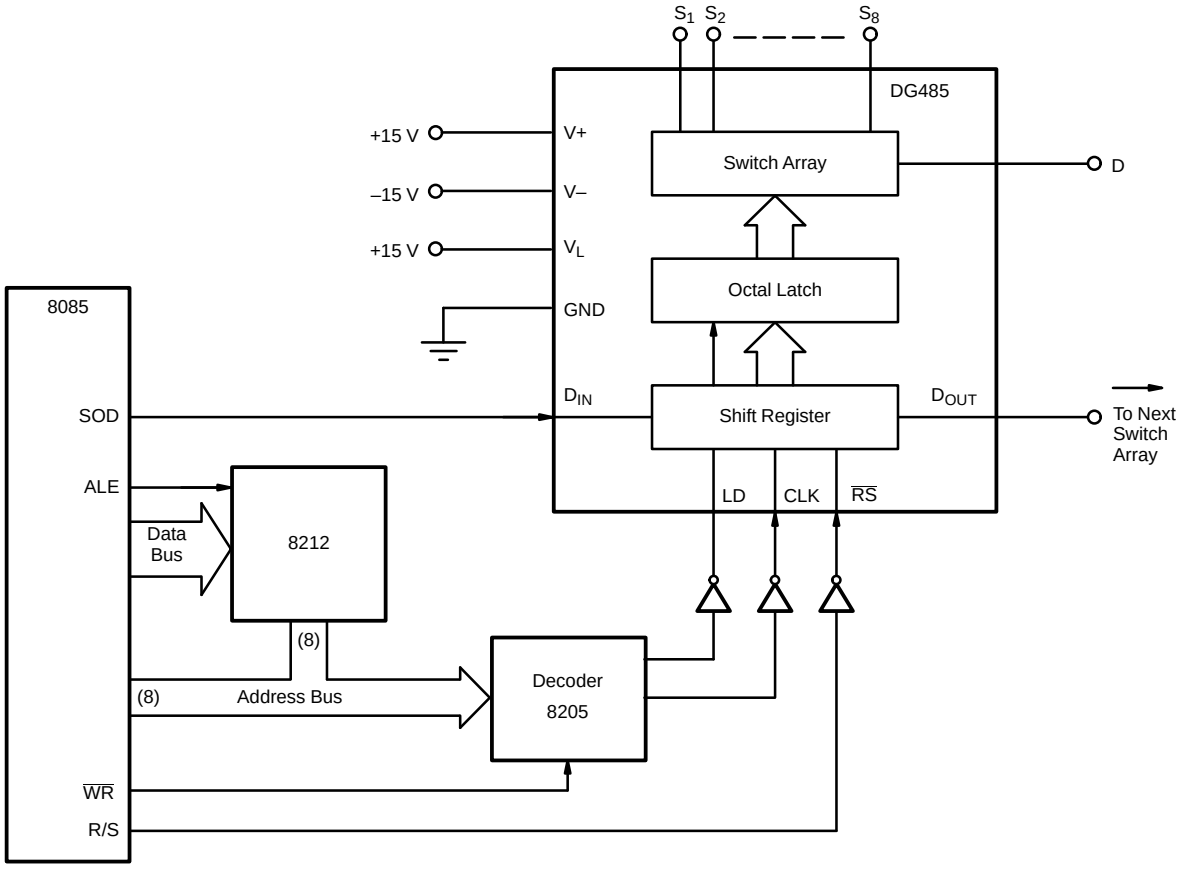


FIGURE 3. The DG485 Simplifies Analog Signal Control With a Serial Data Bus. The Input Shift Register in the DG485 Receives Switch On/Off-State Data Directly From the Serial Data (SOD) Line from the Microprocessor.

Switch Array with Improved Speed and Accuracy

In addition to being a useful new function, the DG485 features analog switches with vastly improved performance. They are part of the DG400 family which uses a new silicon-gate CMOS process designed to achieve improved speed, lower power, lower on-resistance, lower leakage, and improved ESD tolerance. These benefits are the result of the inherent reduced overlap parasitic capacitance of silicon-gate CMOS processing.

For comparison of switch performance, key specifications for the industry-standard DG508A eight-channel multiplexer and the DG485 eight-channel array are shown in Table 1. The closest standard IC to the DG485 is the eight-channel DG508A multiplexer. While the DG485 array allows any combination of eight switches to be turned on at one time (compared with the one-of-eight decoding of the multiplexer), it also has improved speed and accuracy with reduced power dissipation. Key specifications for the DG485 array and the DG508A multiplexer are compared in Table 1.

TABLE 1.

Key Specification (@ 25°C)	DG508A 8-Channel Multiplexer	DG485 8-Channel Array
Fabrication Process	44 V Metal-Gate CMOS	44 V Silicon-Gate CMOS
On-resistance ($r_{DS(ON)}$ Max.)	450 Ω	85 Ω
Leakage ($I_{S(off)}$ Max.)	5 nA	1 nA
Switching Time ($t_{(tran)}$ Max.)	1 μs (1000 ns)	200 ns
Power Dissipation (PD Max.)	59 mW (59000 μW)	105 μW
ESD Tolerance	500 V	4000 V

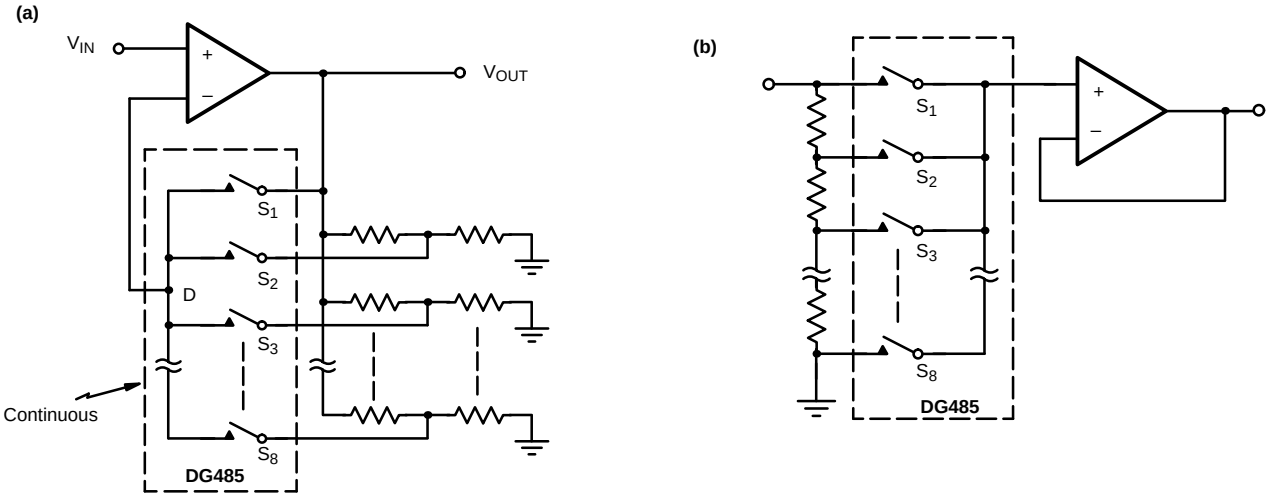


FIGURE 4. Gain Ranging and Attenuator Circuits

Digitally Controlled Signal Conditioning

Input signal conditioning functions like gain ranging, programmable attenuation, and variable filter time constant circuits have one thing in common — they use analog switches for selecting various resistor values. There are many ways to create digitally controlled gain stages using CMOS switches.

Using the DG485, as shown in Figure 4a, places the analog switch in series with a high-impedance point, such as the input of an op amp, to eliminate errors associated with switch on-resistance. Additionally, the gain value is determined by the ratio of the gain-setting resistors rather than their absolute value. Thus, the accuracy of the gain setting is a function of the matching or scaling of the resistors, independent of resistor or analog switch variations. If matched or monolithic resistor arrays are used, excellent gain accuracy and low gain drift is achieved with this architecture. The DG485 allows for selection of eight different resistor ratios under serial control, and its any-combination-of-eight architecture also allows 255 different parallel combinations of resistor ratios for additional gain ranges.

A variation on this theme, shown in Figure 4b, provides programmable attenuation. Again, the analog switches are placed in series with a high-impedance point (the op amp input) to eliminate the effect of switch resistance variations. Attenuation values are selected according to the ratio of the resistors in the string.

Digitally Controlled Filter

The programmable filter circuit shown in Figure 5 selects resistors rather than capacitors to change the RC time constant of the low pass. This is a useful function at the input of a data acquisition or digital signal processing system which allows the processor to adjust the corner frequency of its anti-aliasing filter if various sample rates are being used. Only one capacitor is required, and resistors (which are generally low in cost and easier to specify for accuracy and ratios) are selected with the DG485 to generate different filter characteristics. Resistors that are matched to the ones in the feedback loop are switched at the input of the integrator to maintain unity passband gain for any of the four corner frequencies selected.

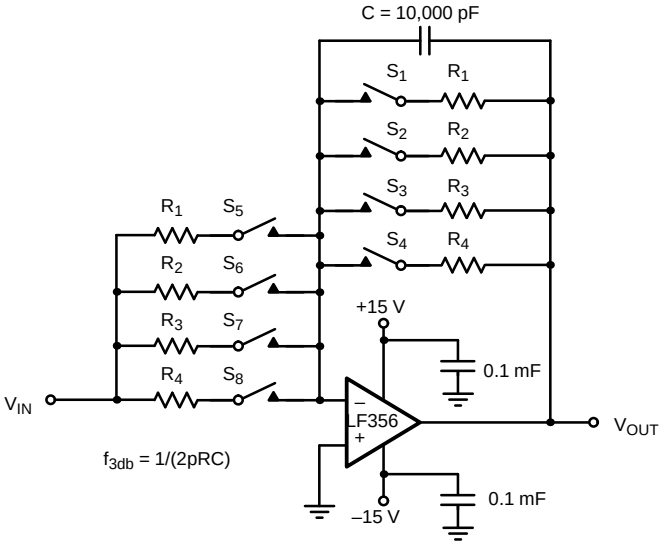
In this filter topology, unlike the gain-ranging circuit shown above, the analog switches are placed in series with the time-constant setting resistors. Therefore, the resistance characteristics of the switches play a significant role in the accuracy of the time constant selection. Switches with low on-resistance are preferred since the time constant of the filter is $(r_{DS(on)} + R_f) \times C$.

If R_f is large, compared to the 85-Ω on-resistance of the DG485, accurate filter break frequencies may be selected via digital serial control. R_{IN} is chosen according to the dc gain requirement of the system. For example, dc unity gain inversion is achieved with $R_{IN} = R_f$. The break frequency, f_{3dB}, is calculated as

$$f_{3dB} = \frac{1}{2\pi RC}$$

The actual measured –3 dB frequencies may vary as much as 10% due to the parasitic drain and source capacitance of the DG485 switches and the variation in on-resistance seen from channel to channel.

Because any combination of the eight switches can be selected, there are a total of sixteen different RC values that can be programmed by using parallel resistor combinations for a wide range of filter roll-offs.



	Code to Shift Register								
	1	2	3	4	5	6	7	8	f_{3db}
R_1 = 1.6 kΩ	1	0	0	0	1	0	0	0	10 kHz
R_2 = 800 Ω	0	1	0	0	0	1	0	0	20 kHz
R_3 = 530 Ω	0	0	1	0	0	0	1	0	30 kHz
R_4 = 400 Ω	0	0	0	1	0	0	0	1	40 kHz

FIGURE 5. Programmable Low Pass Filter

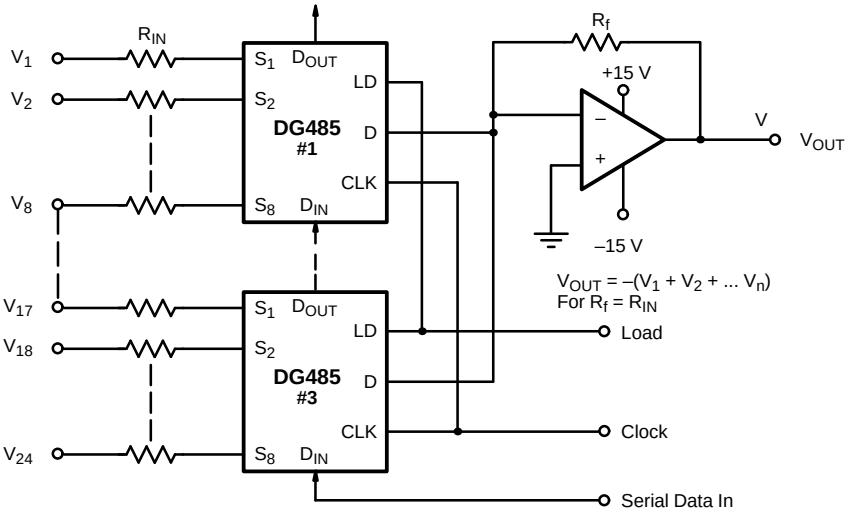


FIGURE 6. The summing-node mixer is frequently used in audio production consoles. Inputs are switched on and off with the summing node of the DG485.

Switching, Selecting, and Summing Multiple Inputs

Frequently a system will process signals from multiple inputs. Time division multiplexing takes samples of each input in successive time intervals. The traditional approach is a multiplexer followed by a sample-and-hold circuit. The DG485 simplifies this function while allowing faster data throughput and higher precision. The channel selection is accomplished with a serial data line, eliminating the latches that are required with a multiplexer, such as the DG508A, when interfacing with the data bus. In addition, the sample-and-hold function is covered by the DG485 with a hold capacitor. The reduced on-resistance and faster transition time of the DG485 allows faster sample acquisition, and the low leakage reduces droop rate.

The Summing-Node Mixer

An eight-channel summing amplifier processes eight inputs in a different way. Like the time-division multiplexer, it selects eight inputs, but rather than sampling each input, it adds the inputs to one another. A classic example is the audio mixer, which sums many audio inputs at the summing node of an op amp to a single output (see Figure 6). For precision, low-noise systems, it is important that the switch resistance remain low because the switches are placed directly in series with the summing resistors and, hence, the analog switches become a factor in the gain and nonlinearity (which results in distortion) of the system. The any-combination-of-eight function of the DG485 allows summing, where the conventional multiplexer function only allows selection of one at a time. In addition, the reduced on-resistance of the DG485 allows a factor of six reduction in the values of the summing resistors, thus reducing noise. The serial control line vastly simplifies addressing in larger mixers. A 24-channel mixer is easily configured without additional address lines using the D_{OUT} (serial data output) feature of the DG485 to daisy-chain the switch arrays (see Figure 6).

The summing-node mixer is a variation of the basic inverting amplifier. If you consider only one channel of the circuit and assume R_{IN} and $R_f >> r_{DS(on)}$ of the DG485 (85 Ω), then the transfer expression is

$$V_{OUT} = -(R_f/R_{IN}) \times V_{IN}$$
or
$$V_{OUT} + -V_{IN} \quad \text{when} \quad R_f = R_{IN}$$

$$V_{OUT} = -\left(\frac{R_f}{R_{IN} + r_{DS(on)}}\right) \times V_{IN}$$

$$V_{OUT} = -(R_f/R_{IN}) \times V_{IN}$$
or
$$V_{OUT} + -V_{IN} \quad \text{when} \quad R_f = R_{IN}$$

If improved gain accuracy or low values of R_f and R_{IN} are required, the effect of $r_{DS(on)}$ cannot be ignored. The expression becomes

$$V_{OUT} = -\left(\frac{R_f}{R_{IN} + r_{DS(on)}}\right) \times V_{IN}$$

Placing a dummy “on” switch from the DG485 into the feedback loop in series with R_f will provide an $r_{DS(on)}$ term in the numerator of the expression.

$$V_{OUT} = \frac{-(R_f + r_{DS(on)})}{R_{IN} + r_{DS(on)}} \times V_{IN}$$

or for $R_f = R_{IN}$

$$V_{OUT} = -V_{IN}$$

When all channels are included, super position gives

$$V_{OUT} = -(V_1 + V_2 + \ldots V_n)$$

for n inputs.

Crosspoint Arrays

An audio crosspoint array provides interconnection between many inputs and many outputs. The serial data addressing feature of the DG485 simplifies the control of a high-quality audio-frequency crosspoint array, such as the one shown in Figure 7. This eight-input, four-output crosspoint uses four DG485s. Cross connection is directly controlled by a 32-bit serial-control word by taking advantage of the DG485's serial-data output pin. By daisy-chaining the switch arrays, the control data is sent through an effective 32-bit shift register, the contents of which are latched into the 32-bit address register on a LD command which is common to all four DG485s. The CLK and $\overline{RS}$ functions are also shared by all four chips.

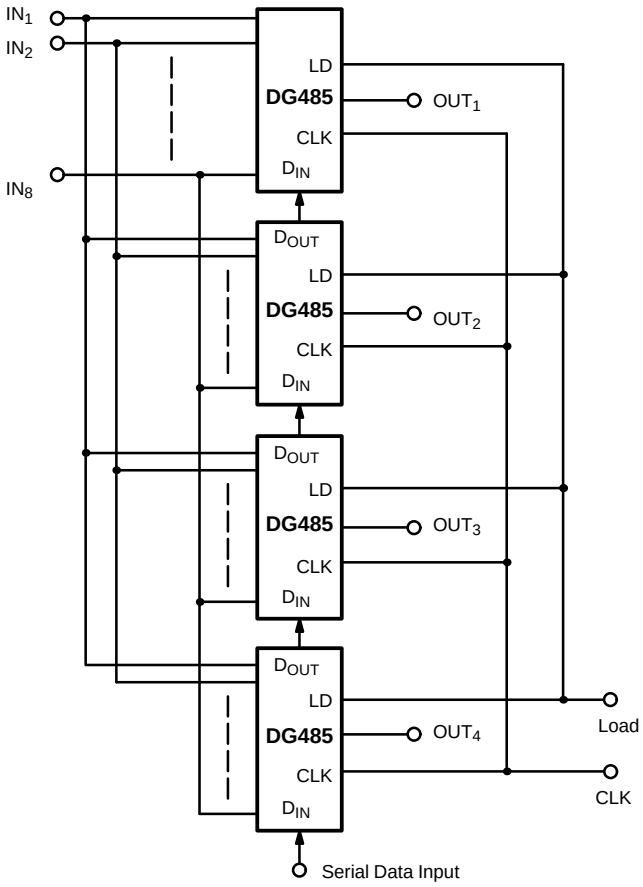


FIGURE 7. An Eight-byFour Audio Crosspoint